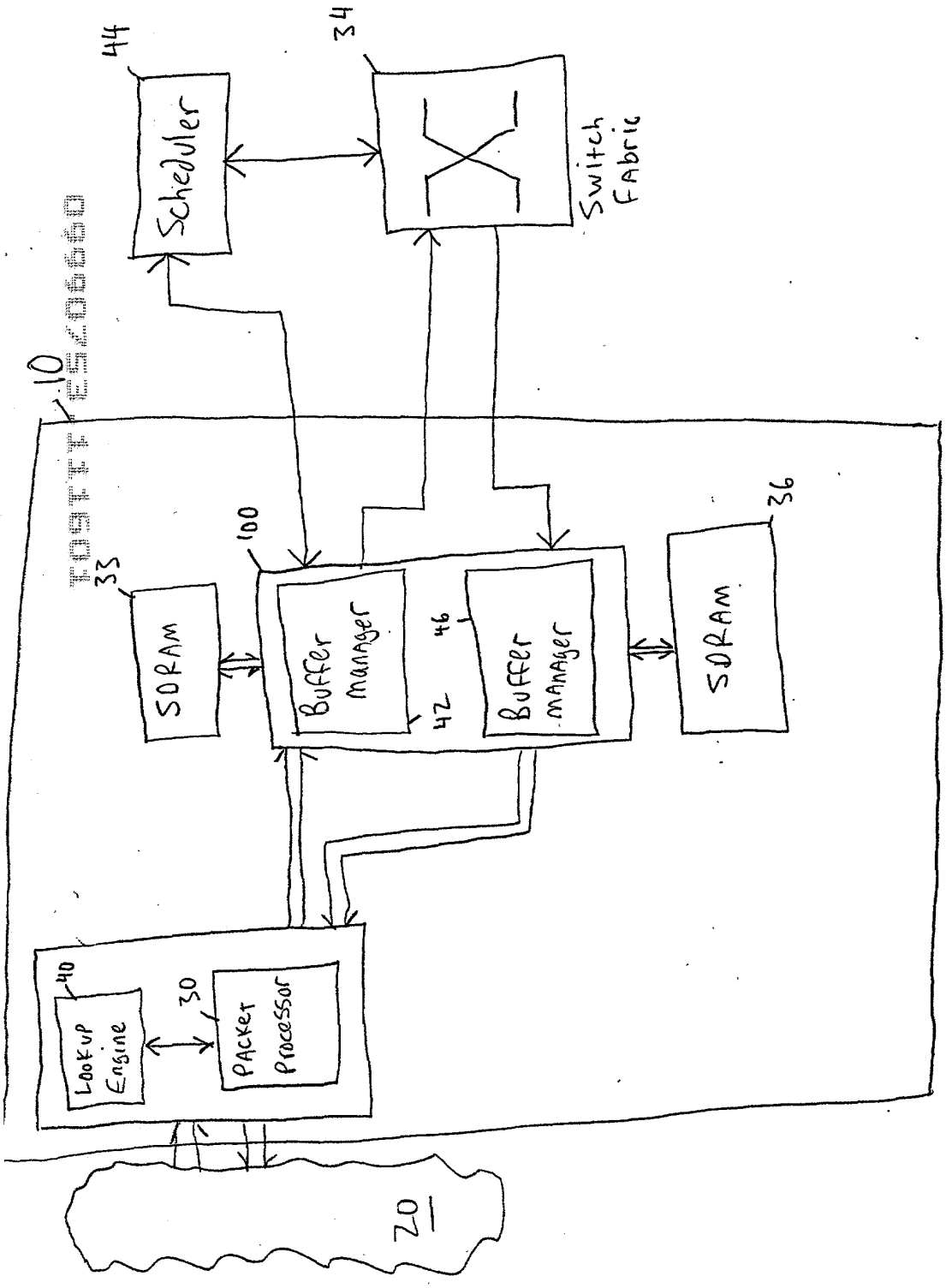

44
Scheduler
34
Switch Fabric
10
33
SDRAM
100
Buffer Manager
46
42
Buffer Manager
36
SDRAM
40
Lookup Engine
30
Packet Processor
20

Fig 1

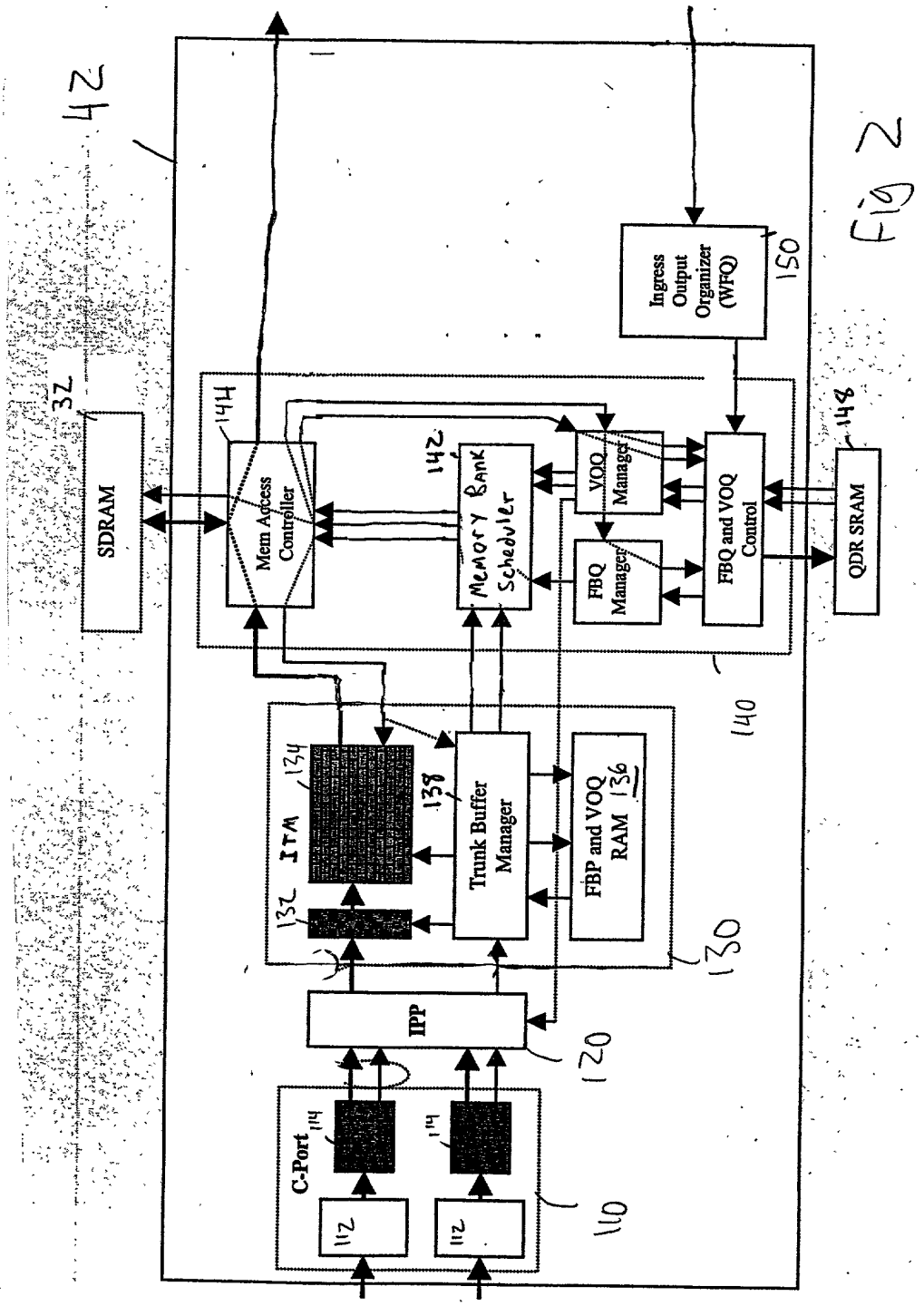

42
32
SDRAM
144
Mem Access Controller
142
Memory Bank Scheduler
VOQ Manager
FBQ Manager
FBQ and VOQ Control
148
QDR SRAM
Ingress Output Organizer (WFQ)
150
140
134
IRM
132
138
Trunk Buffer Manager
FBP and VOQ RAM 136
130
IPP
120
C-Port
114
112
110

Fig 2

EXPRESS MAIL NO. EL 709 690 690

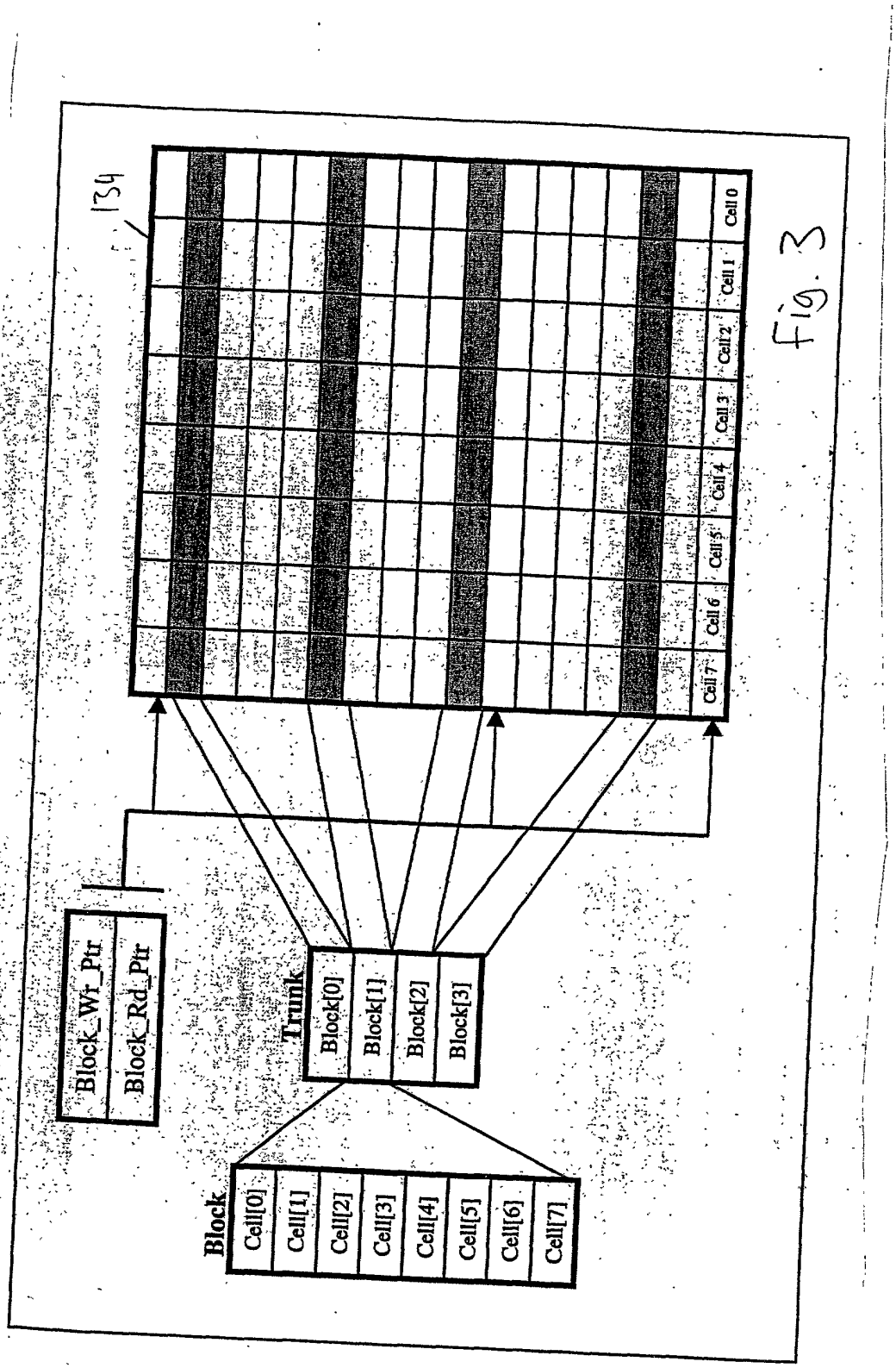


Fig. 3

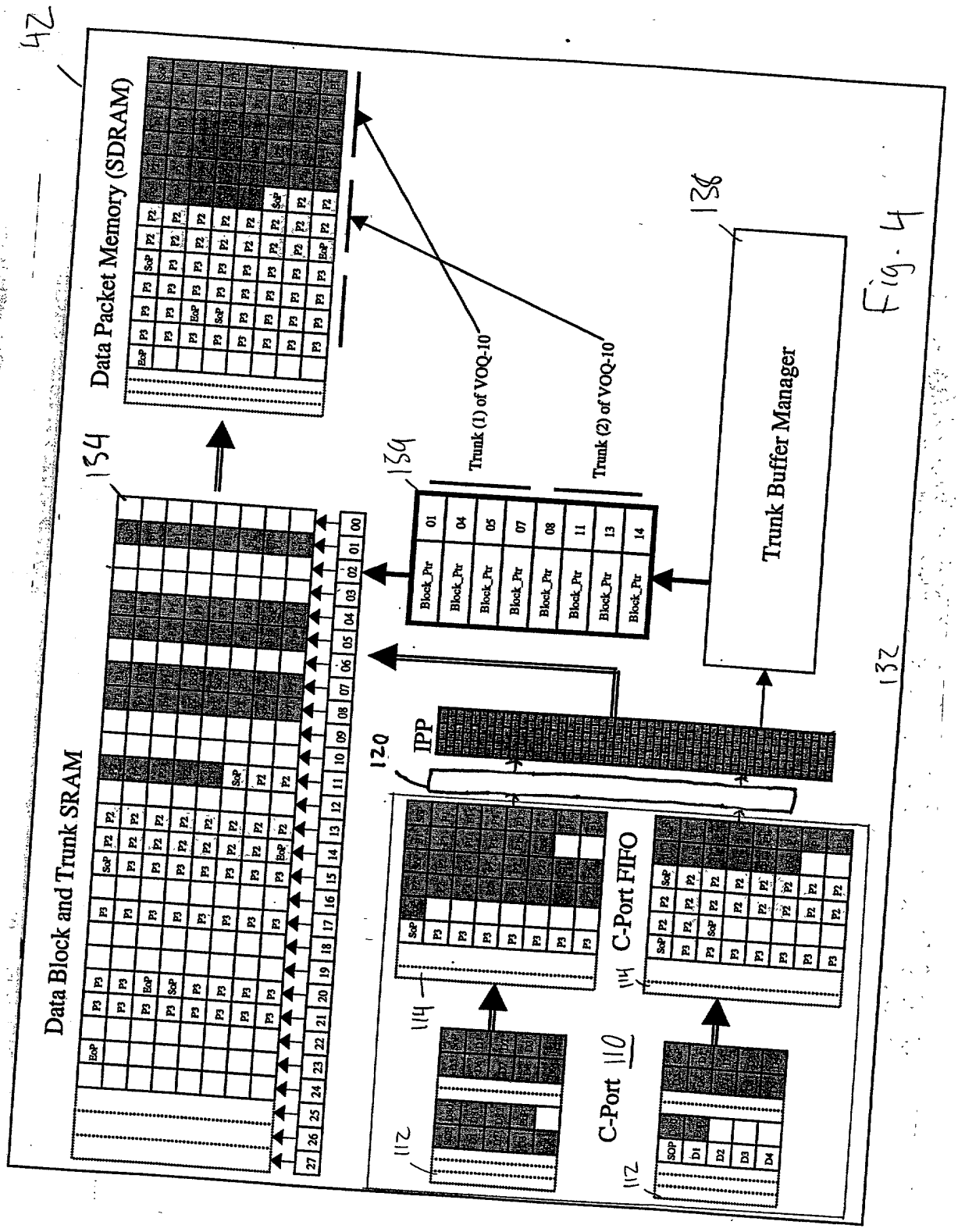

42
Data Packet Memory (SDRAM)
Trunk (1) of VOQ-10
Trunk (2) of VOQ-10
Trunk Buffer Manager
Data Block and Trunk SRAM
IPP
C-Port FIFO
C-Port
SOP
D1
D2
D3
D4
Block_Ptr
01
04
05
07
08
11
13
14
00
01
02
03
04
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27

Fig. 4

Copyright 2003

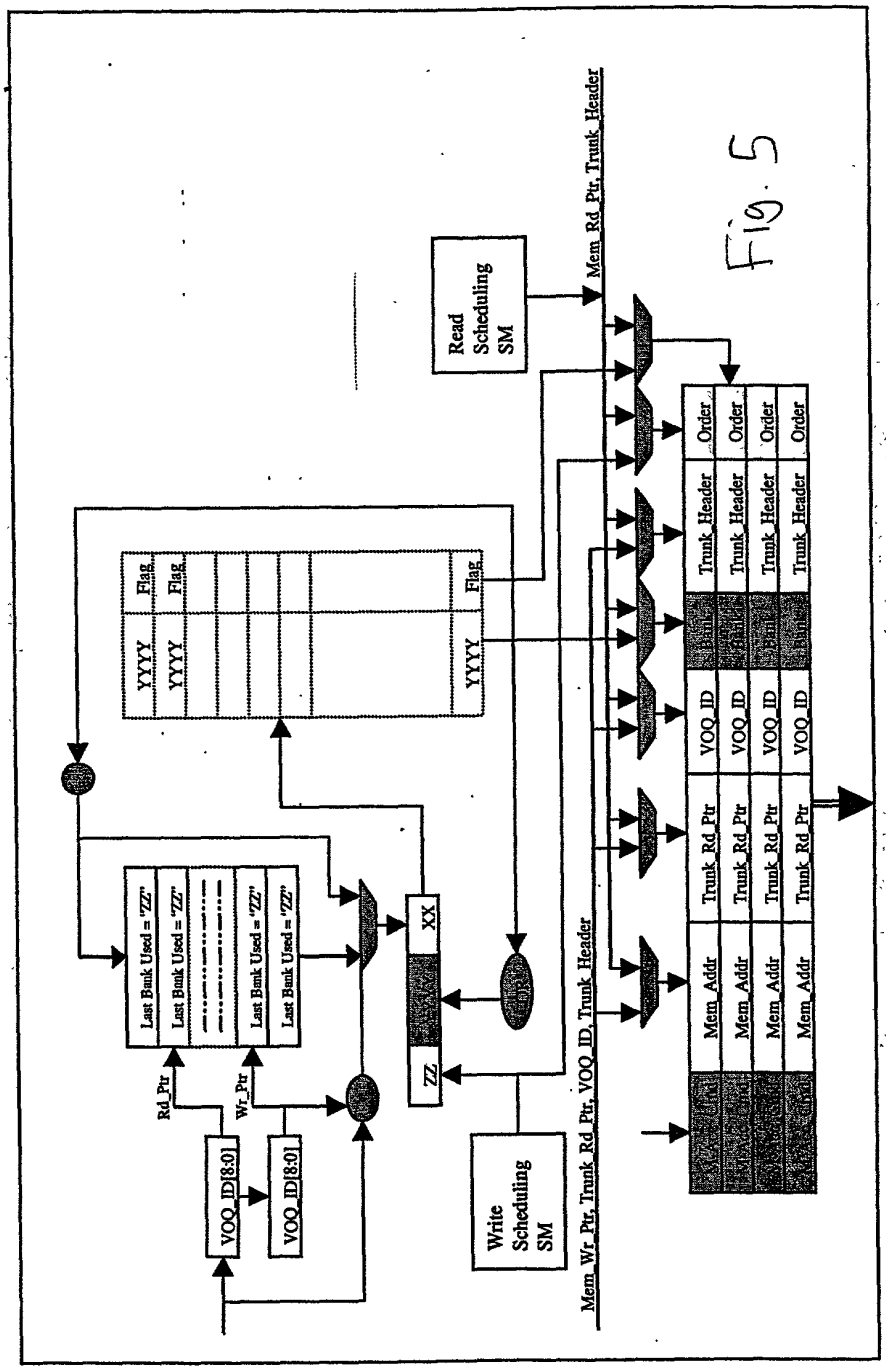


Fig. 5

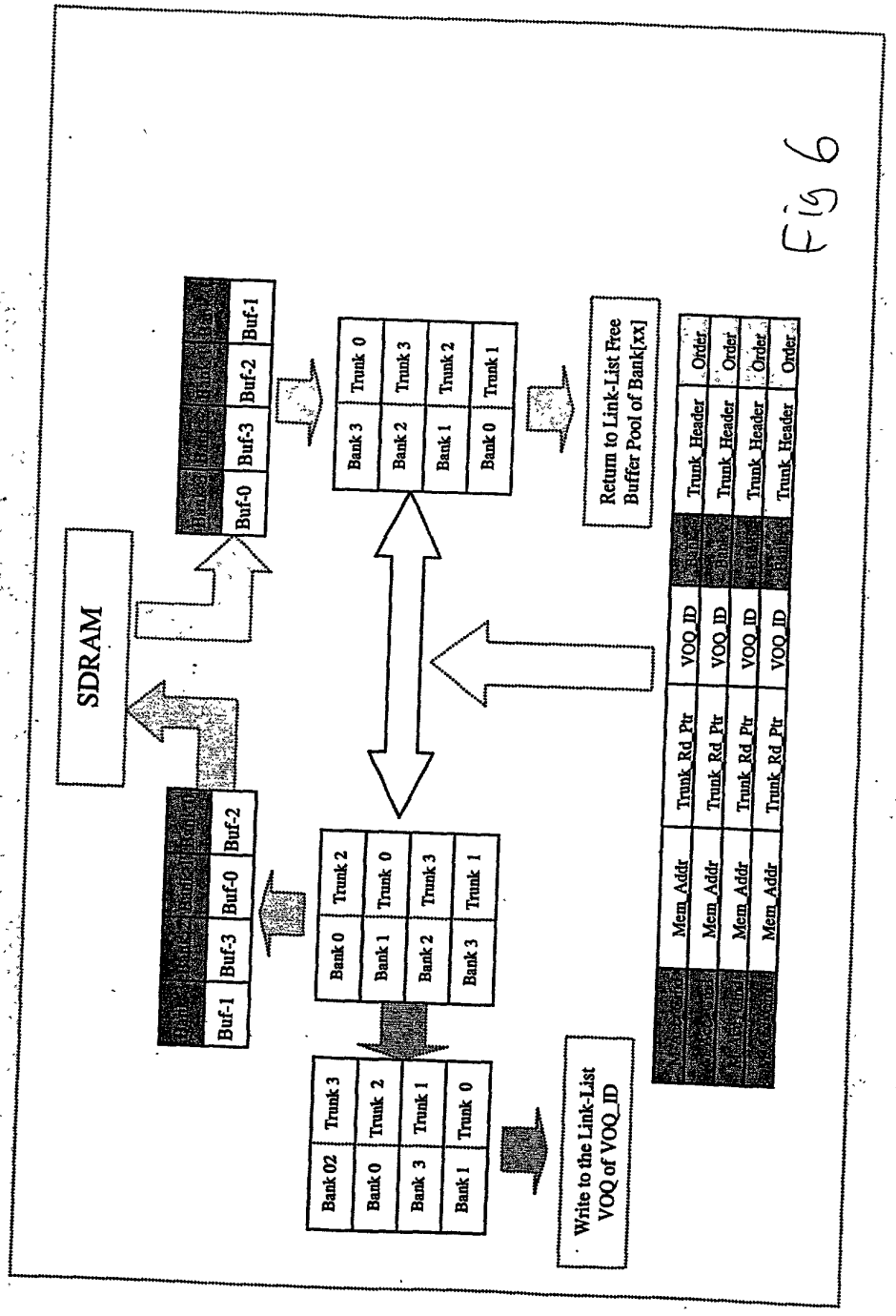

SDRAM
Buf-1
Buf-3
Buf-0
Buf-2
Bank 0
Bank 1
Bank 2
Bank 3
Trunk 2
Trunk 0
Trunk 3
Trunk 1
Bank 02
Bank 0
Bank 3
Bank 1
Trunk 3
Trunk 2
Trunk 1
Trunk 0
Write to the Link-List VOQ of VOQ_ID
Return to Link-List Free Buffer Pool of Bank[xx]
Mem_Addr
Trunk_Rd_Ptr
VOQ_ID
Trunk_Header
Order

Fig 6

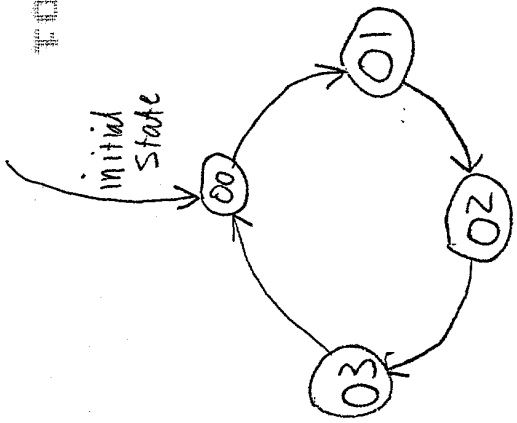


Fig 7A

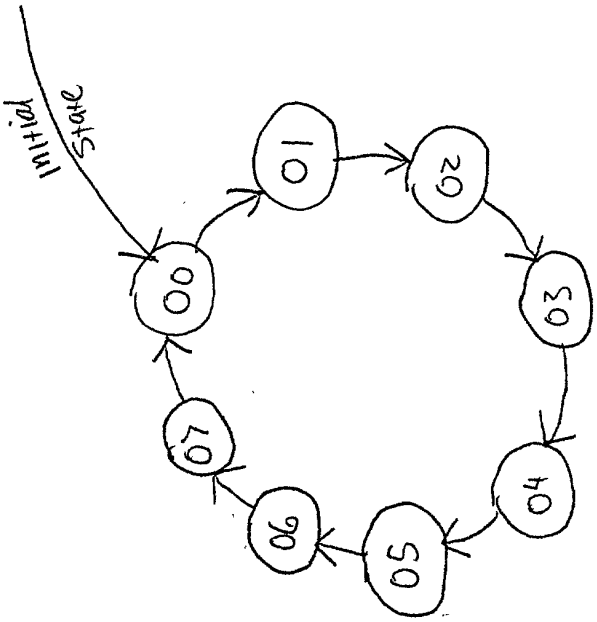


Fig. 7B

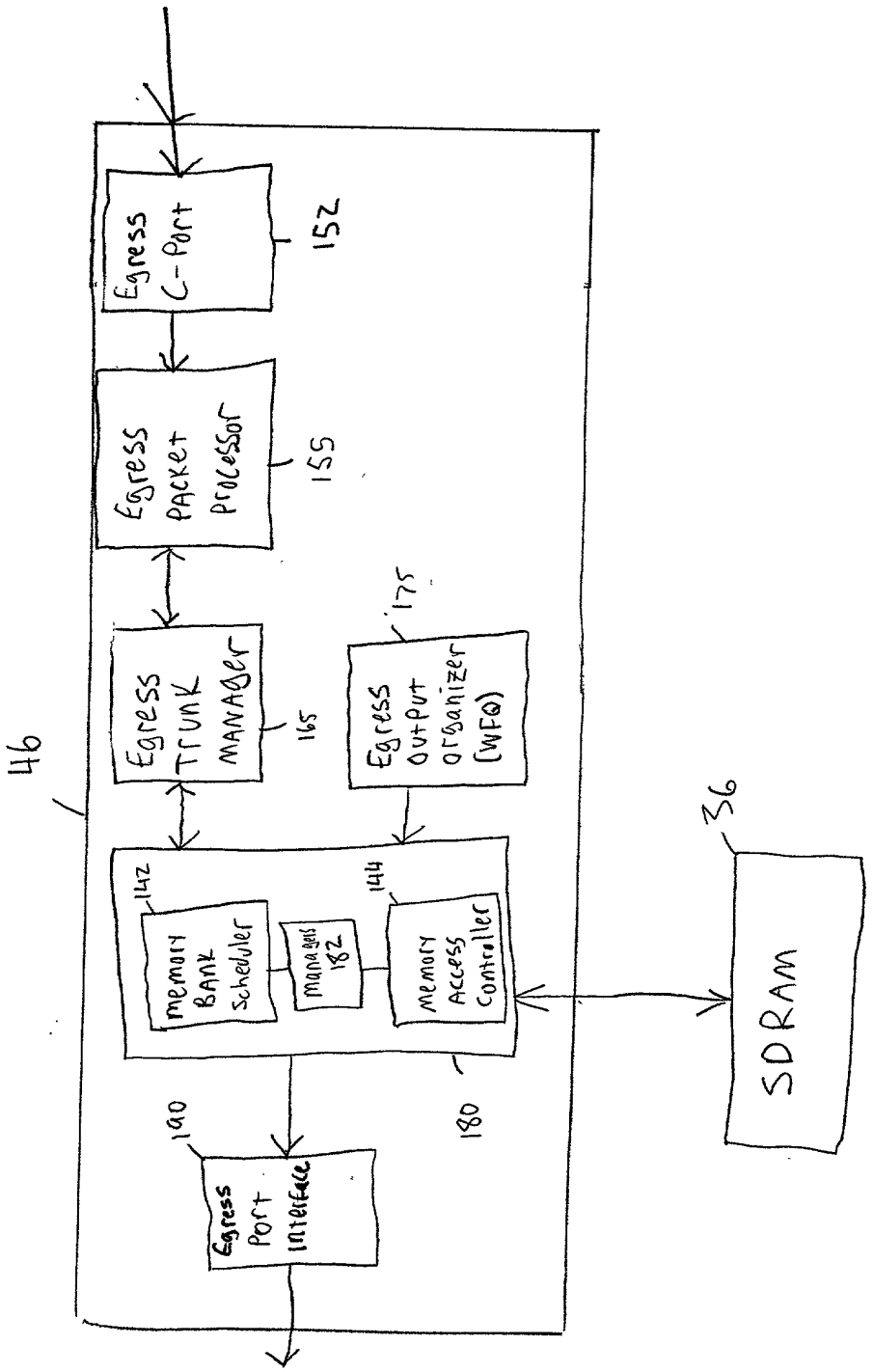

Egress C-Port
152
Egress Packet Processor
155
Egress Trunk MANAGER
165
175
Egress Output Organizer (WFQ)
46
142
memory Bank Scheduler
Manager 182
144
Memory Access Controller
180
36
SDRAM
190
Egress Port Interface

Fig 8

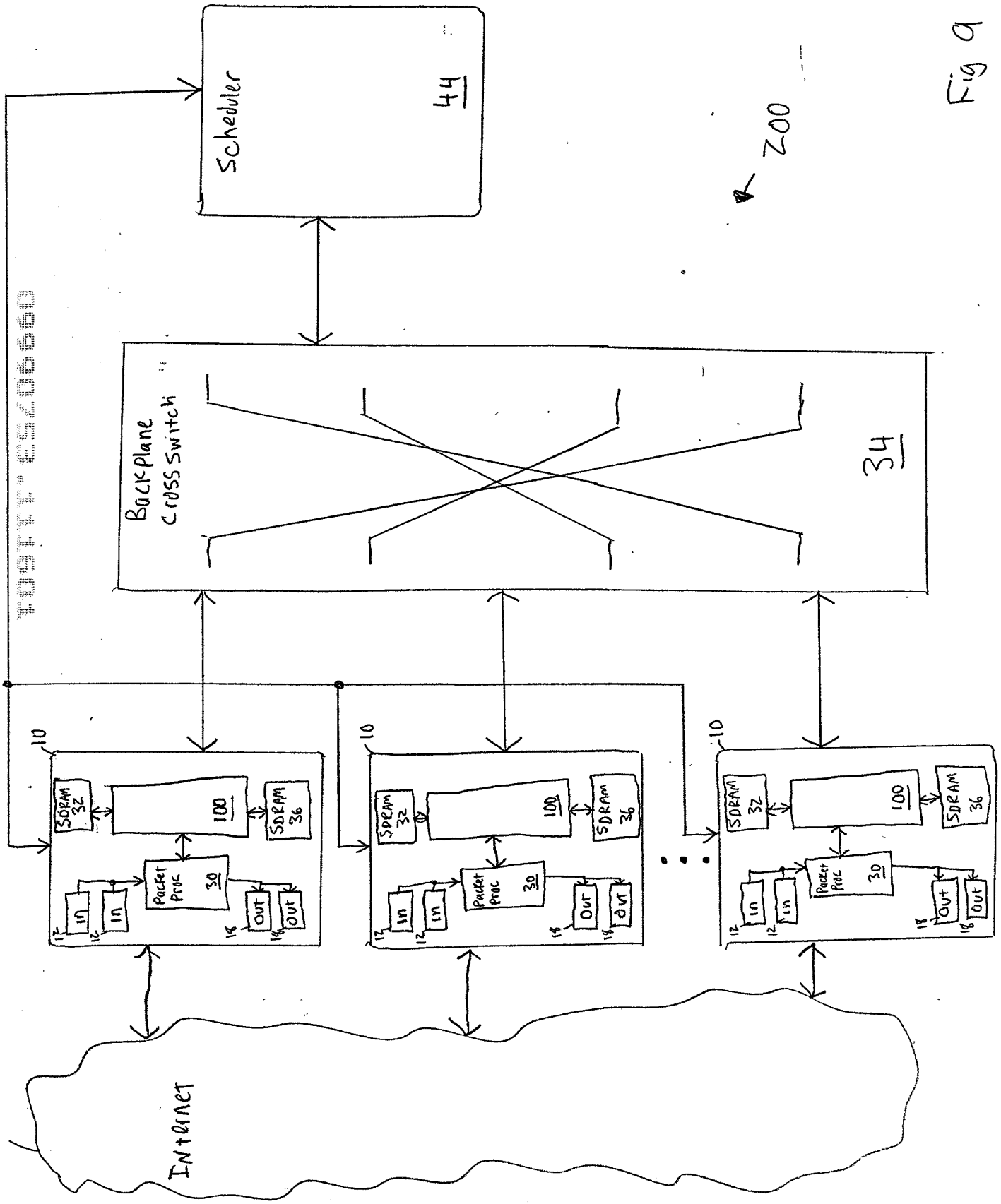
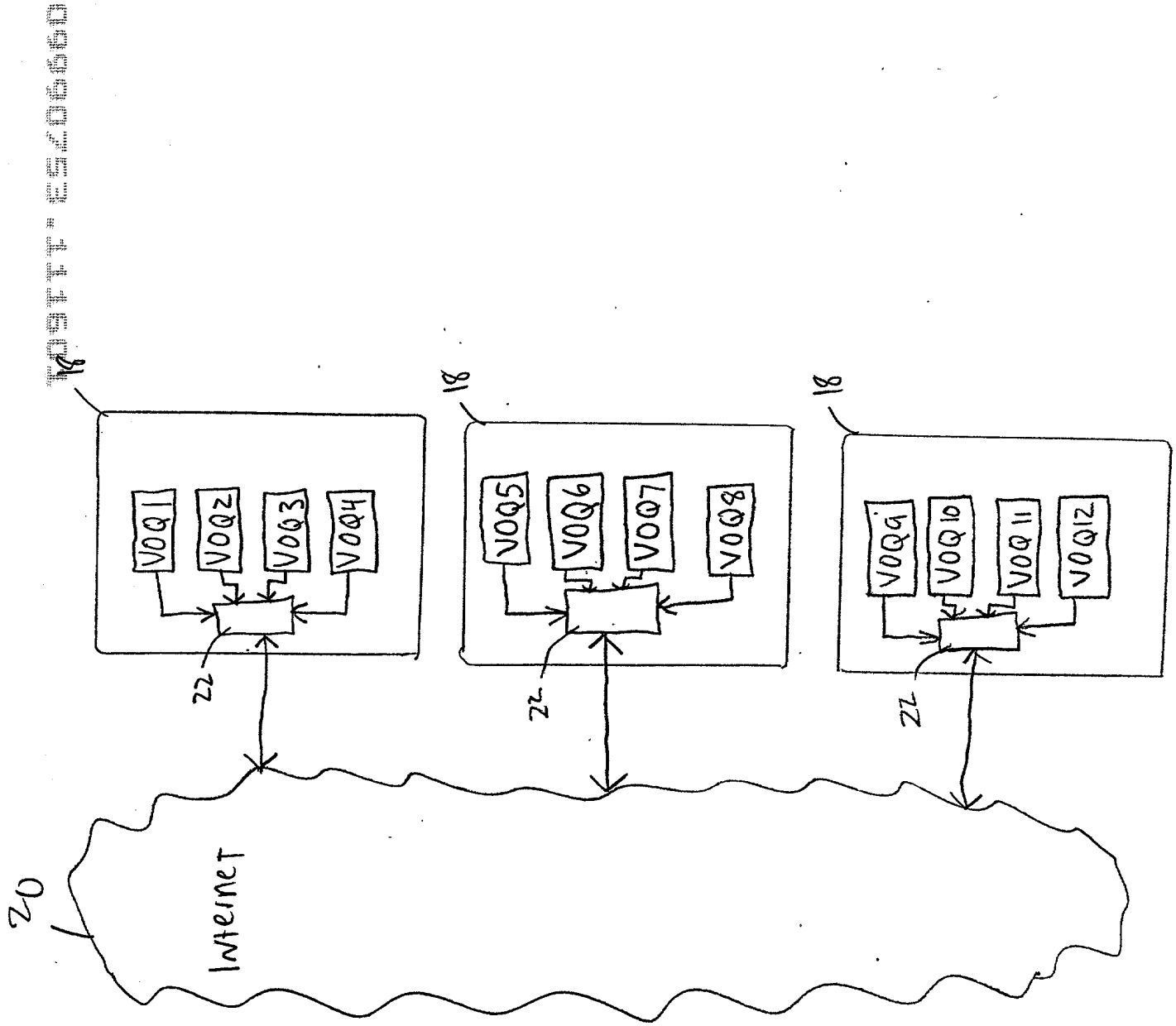

Scheduler
44
200
Backplane
Cross Switch
34
10
SDRAM
32
100
SDRAM
36
Packet
Proc
30
In
Out
12
14
16
18
Internet
20

Fig 9

Fig 10


18
18
18
VOQ1
VOQ2
VOQ3
VOQ4
VOQ5
VOQ6
VOQ7
VOQ8
VOQ9
VOQ10
VOQ11
VOQ12
22
22
22
20
Internet